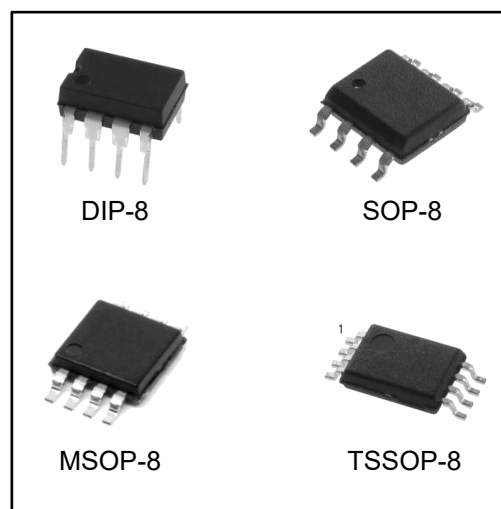## Features

- Low-voltage Operation
- 1.8 (VCC = 1.8V to 5.5V)
- Operating Ambient Temperature: -40°C to +85°C
- Internally Organized 65,536 X 8 (512K),
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1MHZ(5V),400 kHz (1.8V, 2.5V, 2.7V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 128-byte Page (512K) Write Modes
- Partial Page Writes Allowed
- Self-timed Write Cycle (5 ms max)
- High-reliability
- Endurance: 1 Million Write Cycles
- Data Retention: 100 Years
- 8-lead DIP, 8-lead SOP- 8-lead MSOP and 8-lead TSSOP Packages

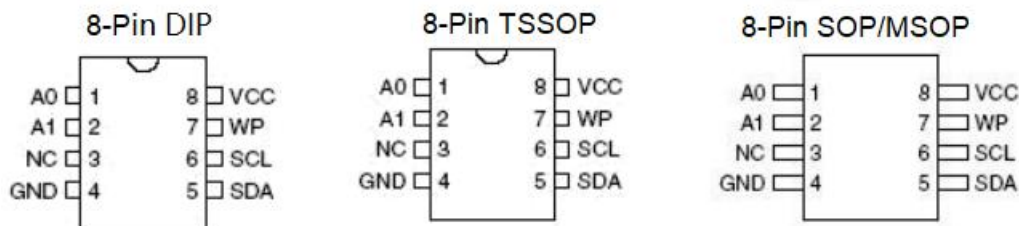DIP-8   SOP-8

MSOP-8   TSSOP-8

General Description

The HX24LC512 provides 524,288 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 65,536 words of 8 bits each. The device's cascadable feature allows up to eight devices to share a common two-wire bus.

The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The devices are available in space-saving 8-pin PDIP, 8-lead JEDEC SOP, 8-lead MSOP, 8-lead TSSOP.

Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
HX24LC512BPG	DIP-8	24LC512B，24LC512	TUBE	2000pcs/box
HX24LC512BDRG	SOP-8	24LC512B，24LC512	REEL	2500pcs/reel
HX24LC512BDRG4	SOP-8	24LC512B，24LC512	REEL	4000pcs/reel
HX24LC512BDGKRG	MSOP-8	LC512B	REEL	3000pcs/reel
HX24LC512BPWRG	TSSOP-8	LC512B	REEL	3000pcs/reel

Pin Configuration

Pin Descriptions

➢ Table 1:Pin Configuration

Pin Designation	Type	Name and Functions
A0-A2	I	Address Inputs
SAD	I/O & Open-drain	Serial Data
SCL	I	Serial Clock Input
WP	I	Write Protect
GND	P	Ground
V_{CC}	P	Power Supply
NC	NC	No Connect

Block Diagram

Pin Descriptions

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is opendraindriven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1, and A0 pins are device address inputs that are hardwired (directly to GND or to Vcc) for compatibility with other HX24LC512 devices. When the pins are hardwired, as many as eight 512K devices may be addressed on a single bussystem. (Device addressing is discussed in detail under "Device Addressing," page 8.) A device is selected when a corresponding hardware and software match is true. If these pins are left floating, the A2, A1, and A0 pins will be internally pulled down to GND. However, due to capacitivecoupling that may appear during customer applications, Fs-Rank recommends always connecting the address pins to a known state. When using a pull-up resistor, Fs-Rank recommendsusing 10kΩ or less.

WRITE PROTECT (WP): The write protect input, when connected to GND, allows normal write operations. When WP is connected directly to Vcc, all write operations to the memory are inhibited.If the pin is left floating, the WP pin will be internally pulled down to GND. However, due to capacitive coupling that may appear during customer applications, Fs-Rank recommends always connecting the WP pins to a known state. When using a pull-up resistor, Fs-Rank recommends using 10kΩ or less.

Table 2: Write Protect

WP Pin Status:	Part of the Array Protected
	HX24LC512
At VCC	Full (512K) Array
At GND	Normal Read/Write Operations

Memory Organization

HX24LC512, 512K SERIAL EEPROM: The 512K is internally organized as 512 pages of 128 bytes each.

Random word addressing requires a 16-bit data word address.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 1 on page 4). Data changes duringSCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precedeany other command (see to Figure 2 on page 5).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence,the stop command will place the EEPROM in a standby power mode (see Figure 2 on page 5).
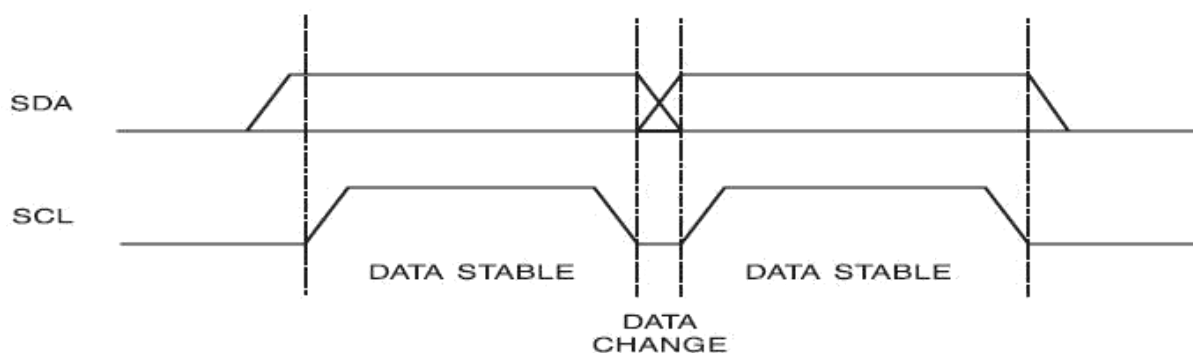
ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle

STANDBY MODE: The HX24LC512 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations
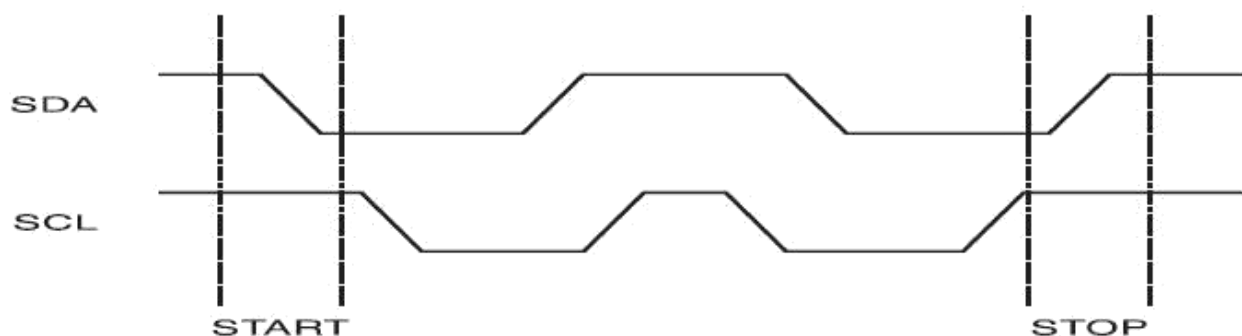
MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can bereset by following these steps:
1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
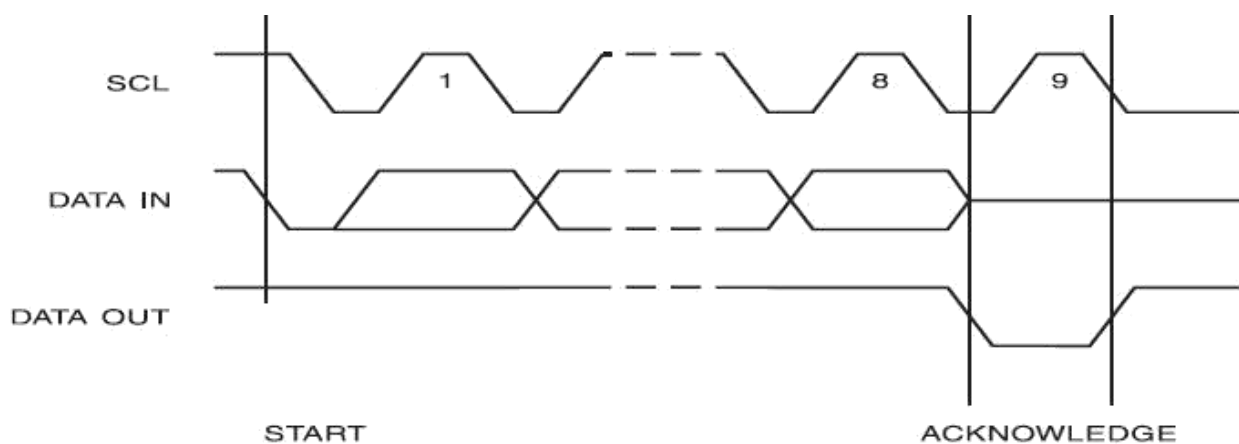3. Create a start condition.

Figure 1. Data Validity

Figure 2. Start and Stop Definition

Figure 3. Output Acknowledge

3. Device Addressing

The 512K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see to Figure 4 on page 4).

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The 512K uses the three device address bits A2,A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A2,A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if thisbit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

DATA SECURITY: The HX24LC512 has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at VCC.

Write Operations

BYTE WRITE: A write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit dataword, the EEPROM will output a "0". The addressing device, such as a microcontroller, then must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 6-2 on page10).

PAGE WRITE: The 512K EEPROM is capable of 128-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 127 more data words. The EEPROM will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 6-3 on page 11).

The data word address lower 7 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the followingbyte is placed at the beginning of the same page. If more than 128 data words are

transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten. The address roll over during write is from the last byte of the current page to the firstbyte of the same page.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a

start condition followed by the device address word. The Read/Write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.
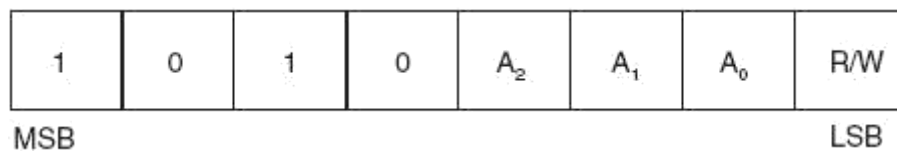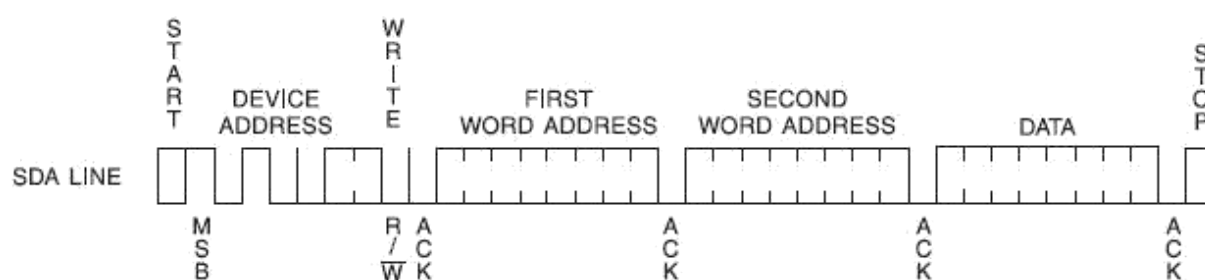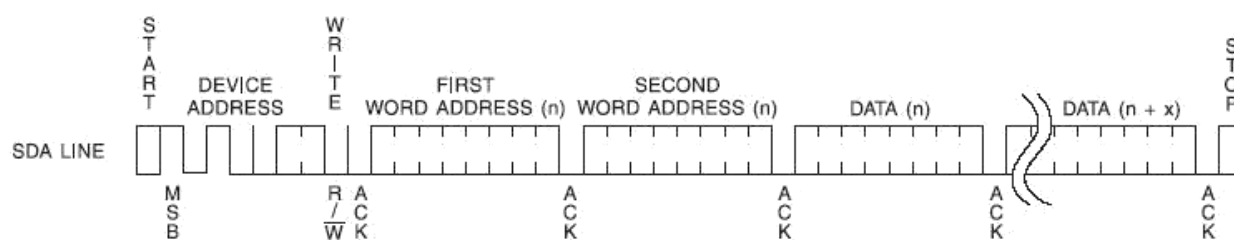
Read Operations

Read operations are initiated the same way as write operations with the exception that the Read/Write select bit in the device address word is set to "1". There are three read operations:current address read, random address read and sequential read.
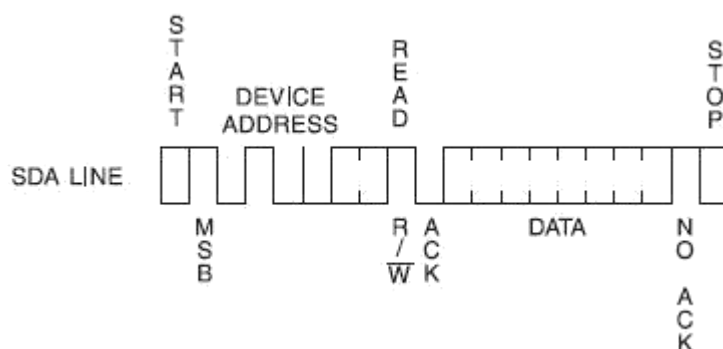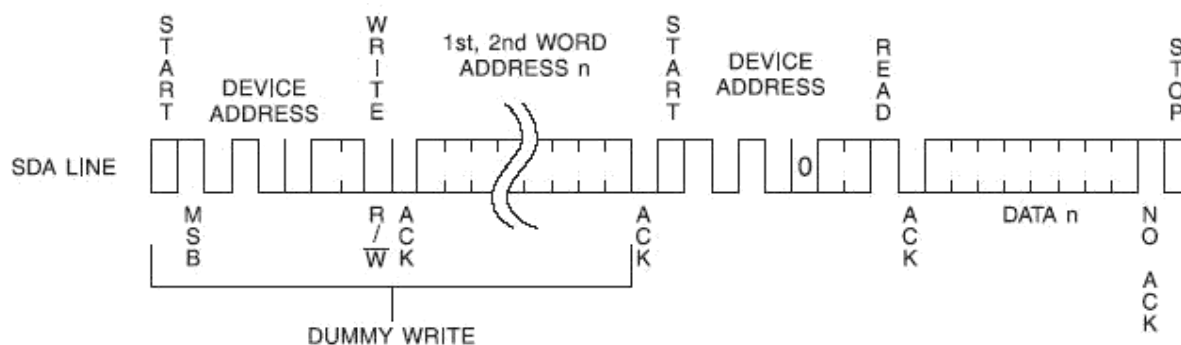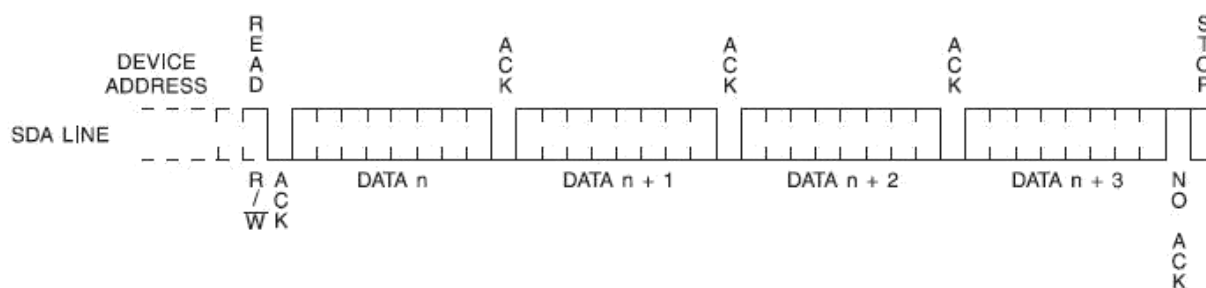
CURRENT ADDRESS READ: The internal data word address counter maintains the last

address accessed during the last read or write operation, incremented by "1". This address staysvalid between operations as long as the chip power is maintained. The address roll over during read is from the last byte of the last memory page, to the first byte of the first page.

Once the device address with the Read/Write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The

microcontroller does not respond with an input "0" but does generate a following stop condition(see Figure 6-4 on page 11).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. Themicrocontroller now initiates a current address read by sending a device address with the Read/Write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a followingstop condition (see Figure 6-5 on page 11).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a randomaddress read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll over and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 6-6 on page 11).

Figure 4. Device Address

Figure 5. Byte Write

Figure 6. Page Write

Figure 7. Current Address Read

Figure 8. Random Read

Figure 9. Sequential Read

Electrical Characteristics

Absolute Maximum Stress Ratings

Symbol	Parameter	Value	Unit
VCC	Supply Voltage	+6.5	V
VO	Input / Output Voltage	GND-0.3 to VCC+0.3	V
Tamb	Operating Ambient Temperature	-40 to +85	°C
Tstg	Storage Temperature	-65 to 125	°C
TL	Lead Temperature (Soldering, 10 seconds)	+245	°C

*Comments

Stresses above those listed under "Absolute Maximum   Ratings"   may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Applicable over recommended operating range from: T_A = –40°C to +85°C, VCC = +1.7V to +5.5V (unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage	V_{CC1}	1.8	-	5.5	V	
Supply Voltage	V_{CC2}	2.5	-	5.5	V	
Supply Voltage	V_{CC3}	2.7	-	5.5	V	
Supply Voltage	V_{CC4}	4.5	-	5.5	V	
Supply Current V_{CC} = 5.0V	I_{CC1}	-	0.4	1.0	mA	READ at 400 kHz
Supply Current V_{CC} = 5.0V	I_{CC2}	-	2.0	3.0	mA	WRITE at 400 kHz
Standby Current V_{CC} = 1.7V	I_{SB1}	-	0.6	1.0	µA	V_{IN} = VCC or VSS
Standby Current V_{CC} = 2.5V	I_{SB2}	-	1.0	2.0	µA	V_{IN} = VCC or VSS
Standby Current V_{CC} = 2.7V	I_{SB3}	-	1.0	2.0	µA	V_{IN} = VCC or VSS
Standby Current V_{CC} = 5.0V	I_{SB4}	-	1.0	5.0	µA	V_{IN} = VCC or VSS
Input Leakage Current	I_{LI}	-	0.10	3.0	µA	V_{IN} = VCC or VSS
Output Leakage Current	I_{LO}	-	0.05	3.0	µA	V_{OUT} = VCC or VSS
Input Low Level	V_{IL}	–0.3	--	VCC x 0.3	V	
Input High Level	V_{IH}	VCC x 0.7	-	VCC + 0.3	V	
Output Low Level VCC =5.0V	V_{OL3}	-	-	0.4	V	I_{OL} = 3.0 mA
Output Low Level VCC =3.0V	V_{OL2}	-	-	0.4	V	I_{OL} = 2.1 mA
Output Low Level VCC =1.7V	V_{OL1}	-	-	0.2	V	I_{OL} = 0.15 mA

Pin Capacitance

Applicable over recommended operating range from TA = 25°C, f = 1.0 MHz, VCC = +1.7V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input/Output Capacitance(SDA)	C$_{I/O}$	-	-	8	pF	V$_{I/O}$ = 0V
Input Capacitance (A0, A1, A2,SCL)	C$_{IN}$	-	-	6	pF	V$_{IN}$ = 0V

AC Electrical Characteristics

Applicable over recommended operating range from TA = –40°C to +85°C, VCC = +1.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Parameter	Symbol	1.7-volt			5.0-volt			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency, SCL	fSCL	-	-	400	-	-	1000	kHz
Clock Pulse Width Low	tLOW	1.2	-	-	0.6	-	-	µs
Clock Pulse Width High	tHIGH	0.6	-	-	0.4	-	-	µs
Noise Suppression Time	tI	-	-	50	-	-	50	ns
Clock Low to Data Out Valid	tAA	0.1	-	0.9	0.09	-	0.9	µs
Time the bus must be free before a new transmission can start	tBUF	1.2		-	0.5	-	-	µs
Start Hold Time	tHD.STA	0.6	-	-	0.25	-	-	µs
Start Setup Time	tSU.STA	0.6	-	-	0.25	-	-	µs
Data In Hold Time	tHD.DAT	0	0	-	0	-	0	µs
Data In Setup Time	tSU.DAT	100	0	-	100	-	0	ns
Inputs Rise Time	tR	-	-	0.3	-	-	0.3	µs
Inputs Fall Time	tF	-	-	300	-	-	300	ns
Stop Setup Time	tSU.STO	0.6	-	-	0.25	-	-	µs
Data Out Hold Time	tDH	50	-	-	50	-	-	ns
Write Cycle Time	tWR	-	5	5	-	-	5	ms
5.0V, 25 C, Byte Mode	Endurance	1M	-	-		-	-	WriteCycles

Note

1. This parameter is characterized and is not 100% tested.

2. AC measurement conditions:

R_L (connects to V_{cc}): 1.3 kΩ(2.5V, 5V), 10 kΩ(1.8V)
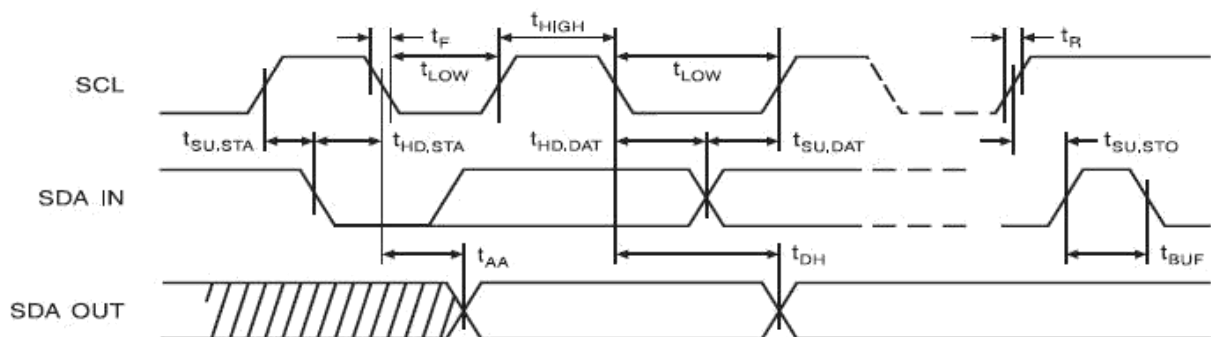
Input pulse voltages: 0.3 V_{cc} to 0.7 V_{cc}

Input rise and fall time: $\leq$ 50 ns

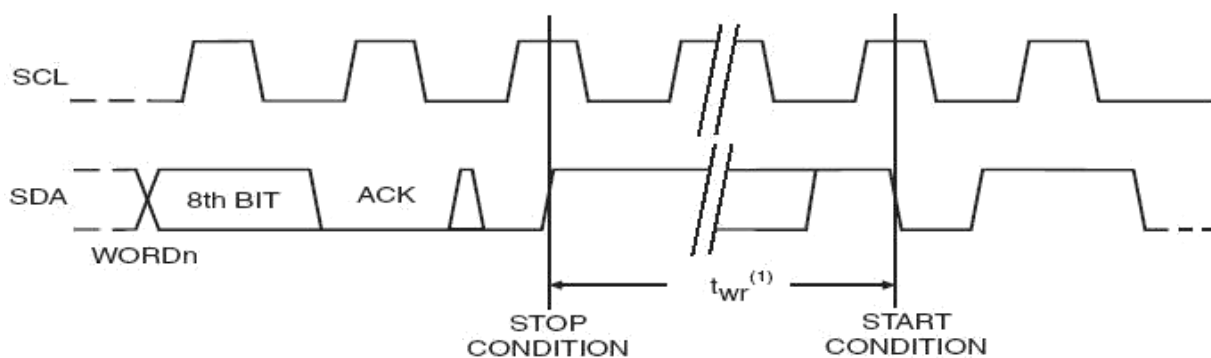Input and output timing reference voltages: 0.5 V_{cc}

The value of R_L should be concerned according to the actual loading on the user's system.
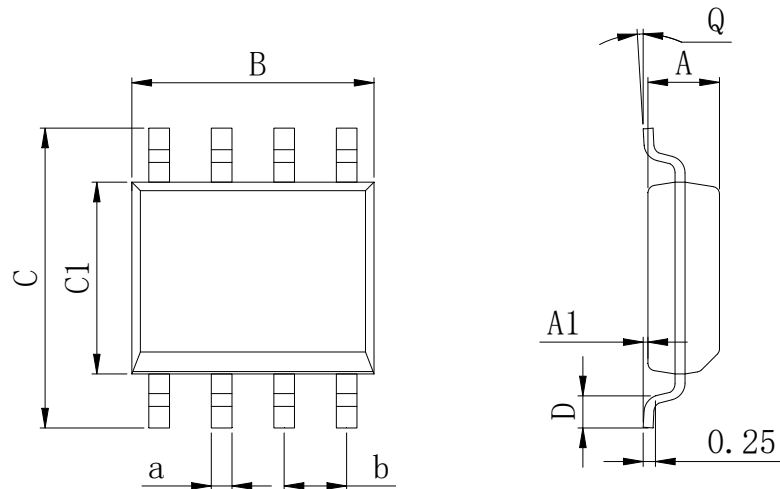
Bus Timing

Figure 10. SCL: Serial Clock, SDA: Serial Data I/O
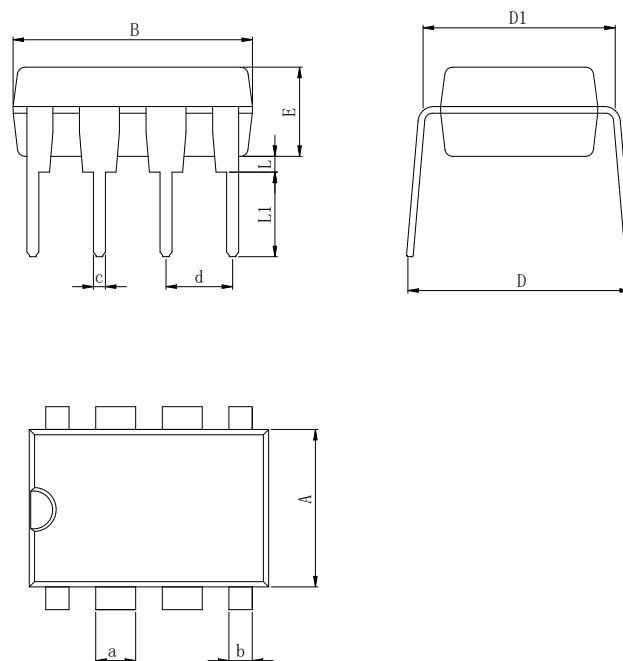

Write Cycle Timing

Figure 11. SCL: Serial Clock, SDA: Serial Data I/O

Note:1.The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

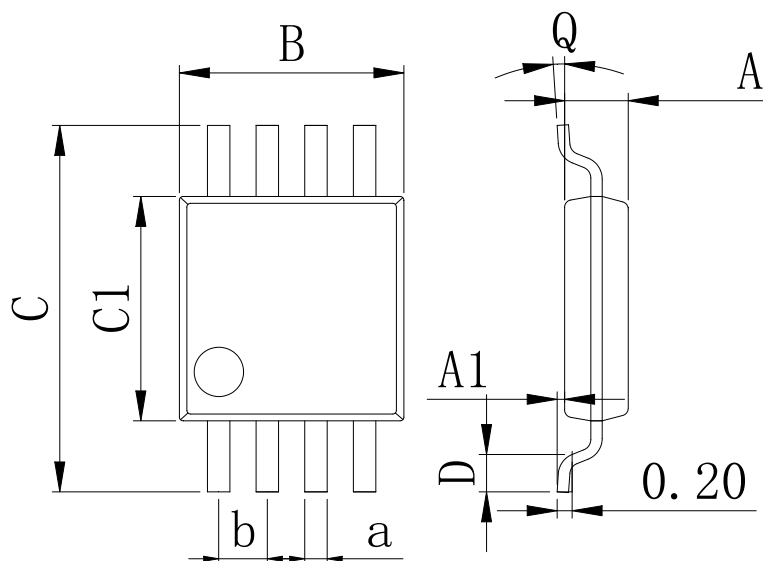# Physical Dimensions

SOP-8

Dimensions In Millimeters(SOP-8)								
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

DIP-8

Dimensions In Millimeters(DIP-8)									
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

Physical Dimensions

MSOP-8

Dimensions In Millimeters(MSOP-8)

Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

TSSOP-8

Dimensions In Millimeters(TSSOP-8)

Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.750	0	2.900	3.900	2.900	0.330	0°	0.300TYP	0.650 TYP
Max:	0.950	0.150	3.100	4.100	3.100	0.470	8°		

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2019-3	New	1-15
V1.1	2023-8	Update encapsulation type、Update Lead Temperature	1、9

IMPORTANT STATEMENT:

Hanschip Semiconductor reserves the right to change its products and services without notice. Before ordering, the customer shall obtain the latest relevant information and verify whether the information is up to date and complete. Hanschip Semiconductor does not assume any responsibility or obligation for the altered documents.

Customers are responsible for complying with safety standards and taking safety measures when using Hanschip Semiconductor products for system design and machine manufacturing. You will bear all the following responsibilities: select the appropriate Hanschip Semiconductor products for your application; Design, validate and test your application; Ensure that your application meets the appropriate standards and any other safety, security or other requirements. To avoid the occurrence of potential risks that may lead to personal injury or property loss.

Hanschip Semiconductor products have not been approved for applications in life support, military, aerospace and other fields, and Hanschip Semiconductor will not bear the consequences caused by the application of products in these fields. All problems, responsibilities and losses arising from the user's use beyond the applicable area of the product shall be borne by the user and have nothing to do with Hanschip Semiconductor, and the user shall not claim any compensation liability against Hanschip Semiconductor by the terms of this Agreement..

The technical and reliability data (including data sheets), design resources (including reference designs), application or other design suggestions, network tools, safety information and other resources provided for the performance of semiconductor products produced by Hanschip Semiconductor are not guaranteed to be free from defects and no warranty, express or implied, is made. The use of testing and other quality control technologies is limited to the quality assurance scope of Hanschip Semiconductor. Not all parameters of each device need to be tested.

The documentation of Hanschip Semiconductor authorizes you to use these resources only for developing the application of the product described in this document. You have no right to use any other Hanschip Semiconductor intellectual property rights or any third party intellectual property rights. It is strictly forbidden to make other copies or displays of these resources. You should fully compensate Hanschip Semiconductor and its agents for any claims, damages, costs, losses and debts caused by the use of these resources. Hanschip Semiconductor accepts no liability for any loss or damage caused by infringement.